Patent Application for

"INTEGRATED MODEM AND LINE-ISOLATION CIRCUITRY WITH HDLC FRAMING AND ASSOCIATED METHOD"

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This application claims priority from Provisional Application Serial No. 60/145,475 to Timothy J. Dupuis, Andrew W. Krone and Mitchell Reid, which was filed July 23, 1999, and is entitled "POWERED SIDE DAA CIRCUIT HAVING MODEM CIRCUITRY."

Technical Field of the Invention

This invention relates to modem architecture for communication lines. More particularly, this invention relates to modem circuitry used in connection with isolation systems for connecting to phone lines.

Background

New generations of consumer appliances like set-top boxes, payphones, vending machines and other systems often require or prefer low-speed data modems. Such modems allow remote hosts to handle billing or other housekeeping functions, or permit "smart" vending machines to call for more supplies. Although typical microprocessor and digital-signal-processor (DSP)-based multimedia chips employed in set-top boxes and other systems are capable of

implementing a low-speed modem, they would do so at an undesirable manufacturing complexity and expense.

Prior modem architectures typically included multiple integrated circuits for handling modem processing and communication line termination. In particular, one or more digital-signal-processor chips have been coupled to analog-front-end circuitry, which in turn has been connected to line termination circuitry across a transformer isolation barrier. Such modem architectures suffer from numerous disadvantages.

Summary of the Invention

The present invention provides an improved modem architecture and associated method that integrate modem and line-isolation circuitry so as to achieve modem functionality and system-side isolation functionality on a single integrated circuit while also providing a modem interface that allows synchronous modem transmission protocols to be implemented through an asynchronous serial interface. For example, one such type of synchronous modem transmission protocol is the HDLC (high-level data link control) protocol. According to the techniques disclosed herein, data and control information of an HDLC protocol may be presented at the transmit and receive pins of a modem/system side DAA through a UART even though the UART may be an asynchronous serial receiver transmitter. Thus, both transmit and receive data transfers of a serial modem protocol may be implemented through an asynchronous serial interface.

In one embodiment, a method of isolating a telephone line is provided. The method may include providing modem circuitry, providing system side line isolation circuitry, integrating the modem circuitry and system side line isolation circuitry within a single integrated circuit, the single integrated circuit configured to communicate through an isolation barrier. The method may further include providing an asynchronous serial port on the single integrated circuit, and configuring the single integrated circuit to transfer data of a synchronous modem transmission protocol through the asynchronous serial port.

In another embodiment, a method of transferring information between a modem circuit and an external interface is disclosed. The method may include providing data of a synchronous modem transmission protocol to an asynchronous serial pin, and transferring the data of the synchronous modem transmission protocol through the asynchronous serial pin in an asynchronous manner.

Yet another embodiment includes a method of transferring data between modem circuitry and an interface. The method may comprise providing the modem circuitry within an integrated modem and system side line isolation circuit, and providing the integrated modem and system side line isolation circuit with an asynchronous serial pin. The method may further include providing data of a synchronous modem transmission protocol to the asynchronous serial pin, and transferring the data of the synchronous modem transmission protocol through the asynchronous serial pin.

Another embodiment is directed towards circuitry for transferring data of a synchronous modem transmission protocol. The circuitry may include an integrated modem and line-isolation circuit. The circuitry may further include an asynchronous serial pin, the asynchronous serial pin being an input or output pin of the integrated modem and line-isolation circuit. The circuitry may also include means to enable transfer of data of the synchronous modem transmission protocol through the asynchronous serial pin.

In another embodiment, an integrated line isolation circuit is provided. The circuit may comprise modem circuitry and system side line isolation circuitry integrated within the line isolation circuit. The circuit may further comprise an asynchronous serial interface pin coupled to the modem circuitry and the system side line isolation circuitry, the integrated line isolation circuit configured to transfer data of a synchronous modem transmission protocol through the asynchronous serial interface pin.

Description of the Drawings

It is noted that the appended drawings illustrate only exemplary embodiments of the invention and are, therefore, not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

FIG. 1A is a block diagram of an embodiment for a combined modem and line-isolation system according to the present invention.

FIG. 1B is a more detailed block diagram of an embodiment, including an example pin-out configuration, for the combined modem and line-isolation system according to the present invention.

FIG. 2A is an example block diagram of an external device connecting to the system-side line-isolation integrated circuit of the line-isolation system according to the present invention.

FIG. 2B is a diagram of a 9-bit communication sequence that may be used to control when the modem circuitry within the system-side line-isolation integrated circuit is in command mode or data mode.

FIG. 3A is a block diagram of an embodiment with path control circuitry for the system-side line-isolation integrated circuit of the line isolation system according to the present invention.

FIGS. 3B-3E are block diagrams of example embodiments for data flow and processing paths that may be selected through the path control circuitry of FIG. 3A.

FIG. 4A is a diagram of a communication sequence that may be utilized to transmit raw data to and from the system-side line-isolation integrated circuit.

FIG. 4B is a block diagram for the receive path digital-signal-processor (DSP) circuitry for the system-side line-isolation integrated circuit of a line isolation system according to the present invention.

FIG. 4C is a block diagram for the transmit path DSP circuitry for the system-side line-isolation integrated circuit of a line isolation system according to the present invention.

FIG. 5 is a block diagram of an embodiment for the line-side line-isolation integrated circuit of the line-isolation system according to the present invention.

FIGS. 6A and 6B are timing diagrams for utilizing the asynchronous interface disclosed herein to transmit and receive data of a synchronous modem protocol.

Detailed Description of the Invention

FIG. 1A is a block diagram of an embodiment for a combined modem and line-isolation system 150 according to the present invention. This combined modem and line-isolation system 150 includes a system-side line-isolation integrated circuit (IC) 100 and a line-side line-isolation integrated circuit (IC) 102. In the embodiment shown, the system-side line-isolation IC 100

includes integrated modem circuitry and circuitry providing system-side direct access arrangement (DAA) functionality. In the embodiment shown, the line-side line-isolation IC 102 includes circuitry providing line-side DAA functionality. The system-side line-isolation IC 100 communicates to external circuitry through the communication interface 106. The line-side line-isolation IC 102 communicates to the communication line through interface 112. It is noted that the communication line may be a desired medium and may be, for example, a telephone line.

The system-side line-isolation IC 100 and the line-side line-isolation IC 102 communicate digital information across an isolation barrier 104 through line interfaces 108 and 110, respectively. The isolation barrier 104 may be a capacitively isolated barrier, including one or more capacitors, and may also include a transformer or other isolation device, as desired. In addition, line-isolation systems and associated capacitively isolated barriers are disclosed in U.S. Patent No. 5,870,046 entitled "Analog Isolation System with Digital Communication Across a Capacitive Barrier," and U.S. Patent Application Serial Number 09/035,175 entitled "Direct Digital Access Arrangement Circuitry and Method for Connecting to Phone Lines," which are both hereby incorporated by reference in their entirety.

The present invention provides a single integrated circuit solution for a modem and system-side line-isolation circuitry. The modem digital-signal-processing (DSP) functionality has been combined with the system-side line-isolation DSP functionality to provide a DSP engine capable of handling, for example, both digital filter processing needed for phone line DAA functionality and modem processing needed for processing modem algorithms. This

architecture achieves numerous advantages, including: (1) improved power savings by allowing the line-side line-isolation IC to be powered at least in part from the communication line, (2) improved DAA programmability by having a programmable device on the system side of the isolation barrier 104, (3) improved manufacturing and design capabilities by having a digital system-side chip 100 separate from the mixed signal line-side chip 102, and (4) improved DSP efficiency by using a single DSP engine to process both modem algorithms and required digital filters for the analog-front-end circuitry.

A wide range of interface protocols may be utilized to communicate over the external interface 106, including, for example, modem standards, such as V.22 bis (QAM), V.22/Bell 212A 1200 bit/s (DPSK), V.21/Bell 103 300 bit/s (FSK), V.23/Bell 1200 bit/s V.23 with data flow reversing, and V.25-based fast connect. In addition, the modem interface 106 can handle the Security Industry Association's generic digital communication standard, as well as other alarm protocols. The interface 106 may also be, for example, an asynchronous serial interface. If desired, the interface 106 may also be designed as a synchronous serial interface, an asynchronous parallel interface, a synchronous parallel interface, or any other desired interface.

FIG. 1B is a more detailed block diagram of an embodiment for combined modem and line isolation system 150 according to the present invention. The isolation barrier 104 is a capacitively isolated barrier that is connected between external pins of the system-side line-isolation IC 100 and the line-side line-isolation IC 102.

The system-side line-isolation IC 100 includes an isolation interface 164, a digital-signal-processor (DSP) 154, a microcontroller 151, an audio CODEC (COder-DECoder) 152, a clock interface 162, a control interface 160, a UART (Universal Asynchronous Receiver Transmitter) processor 156, and a multiplexer (MUX) 158. The UART processor 156 operates to convert parallel bytes from the microcontroller 151 into serial bits for transmission to and receipt from an external device through the transmit pin TXD and receive pin RXD, respectively. For example, the UART may operate in an 8-bit word format or a 9-bit word format for serial data transmission through the transmit pin TXD and/or the receive pin RXD.

The DSP 154 provides data pump functionality and may be, for example, a 14-bit DSP that performs data pump functions. The microcontroller 151 provides AT command decoding and call progress monitoring and may employ, for example, a 4-bit program word and an 8-bit data word. The clock interface 162 includes a clock generator that accepts a high-frequency (e.g., 4.9152-MHz) master clock input. It also generates all the modem sample rates for supporting the modem standards designed into the system-side line-isolation IC. In addition, the generator provides a 9.6 kHz rate for audio playback.

Pins for the system-side line-isolation IC 100 may include the transmit pin TXD, the receive pin RXD, the reset pin RESET_, the clear-to-send pin CTS_, the clock output pin CLKOUT, crystal oscillator pins XTALI and XTALO, and the analog output pin AOUT. Four other pins may be general purpose programmable input/output pins GPIO1, GPIO2, GPIO3, and GPIO4. Each of these pins may be set up as analog in, digital in, or digital out pins, depending

upon user programming of pin functionality. In particular, the GPIO1 pin may also function as the end of frame pin EOFR for HDLC framing. The GPIO2 pin may provide an analog in pin AIN. The GPIO3 pin may function as an escape pin ESC for controlling command or data modes. And the GPIO4 pin may function as the alert pin ALERT for signaling events such as an intrusion event. Programming and control of the system-side line-isolation IC 100 may be accomplished by sending appropriate commands through the serial interface. For example, commands may be sent by an external integrated circuit that load internal registers within the system-side line-isolation IC 100 that control the operation and functionality of the system-side line-isolation IC 100.

Line-side line-isolation IC 102 includes an isolation interface 166, ring detect and off-hook circuitry 170, and circuitry 168 that includes hybrid and DC termination circuitry as well as analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry. Pins for the line-side line-isolation IC may include a receive input pin RX, filter pins FILT and FILT2 that may set the time constant for the DC termination circuit, a reference pin REF that may connect to an external resistor to provide a high accuracy reference current, a DC termination pin DCT that may provide DC termination for the phone line and an input for voltage monitors, voltage regulation pins VREG and VREG2 that may connect to external capacitors and provide a bypass for an internal power supply, external resistor pins REXT and REXT2 that may provide real and complex AC termination, ring pins RNG1 and RNG2 that may connect through capacitors to "tip" and "ring" to provide ring and caller ID signals across the barrier 104, and transistor connection pins QB, QE and QE2 that may connect to external bipolar hook-switch transistors.

It is noted that the underscore suffix "_" added to pin signals above indicate signals that are active low. It is noted that the active high or active low indications for the external pins of the system-side line-isolation IC 100 and the line-side line-isolation IC 102 are a design choice that may be changed if desired.

FIG. 2A ~~is a example~~ IS AN EXAMPLE block diagram 200 of an external device connected to the system-side line-isolation IC 100 portion of isolation system 150 according to the present invention. In particular, FIG. 2A shows an external microcontroller 202 connected to the system-side line-isolation IC 100. The interface 108 to the isolation barrier 104 is connected to the system-side line-isolation IC 100, and an external communication interface 204 is connected to the microcontroller 202. Also shown in FIG. 2A are the receive pin RXD connections 206, the transmit pin TXD connections 208, the clear-to-send pin CTS_ connections 212, and the escape pin ESC connections 210. In addition, ~~there are an~~ THERE IS AN analog in AIN connection 216 and an analog out AOUT connection 214 coupled to the system-side line-isolation IC 100. It is noted that the microcontroller and/or the system-side line-isolation IC may be connected to other communication lines or buses, for example, to an RS-232 bus through appropriate drive circuitry.

The escape pin ESC 210 allows for rapid control of whether the system-side line-isolation IC 100 is in command or data mode. This escape pin ESC provides a technique for telling the system-side line-isolation IC 100 whether to interpret incoming signals as data or commands. For example, if the microcontroller 202 applies a high logic level to the ESC pin, the modem

circuitry within the system-side line-isolation IC 100 knows that the incoming information is a command. Conversely, if the microcontroller 202 applies a low logic level to the ESC pin, the modem circuitry within the system-side line-isolation IC 100 knows that the incoming information is data. It is noted that these high and low logic levels could be reversed, as desired.

Alternatively, if the UART is operating in a 9-bit word format, one bit of a 9-bit sequence received by the system-side line-isolation IC 100 may be used to identify data mode or command mode. For example, standard modem control may use an 8-bit word format for serial data stream communication. If the modem data pump that is part of the DSP 154 is set to operate at 8-bits and the UART 156 is set to operate at 9-bits, the extra bit applied to the UART 156 may be utilized to identify whether the data input should be treated as data or a command. For example, if the extra bit is a low logic level, the modem circuitry within the system-side line-isolation IC 100 knows that the incoming information is a command. Conversely, if the extra bit is a high logic level, the modem circuitry within the system-side line-isolation IC 100 knows that the incoming information is data. It is noted that these high and low logic levels could be reversed, as desired.

An embodiment for this 9-bit control timing is shown with respect to FIG. 2B for information on the receive RXD lines 254. This timing includes a START bit 256, which is a low logic level for the embodiment in FIG. 2B, and a STOP bit 253, which is a high logic level for the embodiment in FIG. 2B. The logic levels for the START bit 256 and the STOP bit 253 may be selected as desired. As shown in FIG. 2B, the 9th bit in the sequence may be used as a

control flag bit (F) 252 to identify command mode or data mode, with command mode being a logic "1" and data mode being a logic "0", or vice versa. The other 8-bits (D0, D1, D2, D3, D4, D5, D6 and D7) may be the data or command information 250. Thus, the external microcontroller 202 may identify each set of 8-bits of serial data as command data or modem data, depending upon how the 9th bit is set. This information is sent through the RXD pin 206 or the TXD pin 208, for example, by a microcontroller, such as an 8051 microcontroller utilizing an 8-bit data mode. It is noted that the control flag bit may be one of the other bits in the sequence, as desired. It is also noted that the numbers of data bits and the number of control bits may be selected as desired so that N bits of an M-bit word may be used as control bits and M-N bits of an M-bit word may be used as data bits.

In the combined modem and line-isolation system of the present invention, incoming data is digitized within the line-side line-isolation IC 102 on the line-side of the isolation barrier 104. This digital data is then sent across the isolation barrier 104 to the system-side line-isolation IC 100. In turn, data coming from an external device is processed by the system-side line-isolation IC 100 and sent across the isolation barrier 104 as digital information. It is then converted to an analog signal by the line-side line-isolation IC 102. To allow for voice mode applications with the primarily digital processing provided in the system-side line-isolation IC 100, the present invention includes an audio CODEC 152 in the system-side line-isolation IC 100. With this architecture, the present invention provides a single chip solution that combines modem functionality with voice band functionality, so that the user may select either a modem operational mode or a voice operational mode.

FIG. 3A is a block diagram of an embodiment for the system-side line-isolation IC 100 of ~~an~~ combined modem and line isolation system 150 according to the present invention. A controller 151 receives and transmits information through interface 106. The controller 151 communicates with the digital-signal-processor (DSP) 154 through interface 314. The isolation interface 164 controls communication across the isolation barrier 104 through interface 108. The analog in AIN connection 216 and the analog out AOUT connection 214 connect to an analog-to-digital converter (ADC) 312 and a digital-to-analog converter (DAC) 310, respectively. The ADC 312 and the DAC 310 are part of the audio CODEC 152. Furthermore, the DSP circuitry 154 may be used to provide DTMF (dual-tone multi-frequency) decoding and tone generation so that the system-side line-isolation IC 100 may provide DTMF tone generation functionality and DTMF tone detection functionality. In the embodiment shown, for example, DTMF tones may be received from the communication line 112 through interface 108 or from the analog in AIN connection 216. DTMF tones may be transmitted to the communication line 112 through interface 108 or to the analog out AOUT connection 214.

Path control circuitry 306 is controlled by a control signal 330 that may be programmed by the user. The DSP 154 communicates with the path control circuitry 306 through interface 316. The DAC 310 and the ADC 312 communicate with the path control circuitry 306 through interface 320. The isolation interface 164 communicates with the path control circuitry 306 through interface 318. The path control circuitry 306 may be, for example, a plurality of switches controlled by the control signal 330 so that the desired data flow is achieved. The

control signal 330 may be, for example, a multiple bit signal provided by a programmable control register that determines whether each of the plurality of switches is "on" or "off." This programmable control register may be loaded by sending commands through the serial interface that loads to load the control register with the desired control signal.

By controlling the path control circuitry 306, the flow of data within the system-side line-isolation IC 100 may be controlled as desired. For example, data from interface 106 may be output directly through the analog out AOUT connection 214, may be output to the line-side line-isolation IC 102 through the isolation interface 164, or may be output back from the DSP 154 to the interface 106. Data from the analog in AIN connection 216 may be output back through the analog out AOUT connection 214, may be output to the line-side line-isolation IC 102 through the isolation interface 164, and may be output through the DSP 154 to the interface 106. Data from the line-side line-isolation IC 102 across the interface 108 may be output through the DSP 154 to the interface 106, or may be output through the analog out AOUT connection 214.

FIGS. 3B-3E are block diagrams of embodiments for data flow and processing paths that may be selected through the path control circuitry 306 of FIG. 3A. It is noted that other data flow and process paths could be provided, as desired.

FIG. 3B is a block diagram of an embodiment 350 in which data mode operations are desired. The output 316A and the input 316B of the DSP circuitry 154 are connected to the

isolation interface 164 and are also combined to provide an input 320B to the DAC 310. The analog out AOUT 214, therefore, is a combination of the DSP input signal 316B and the DSP output signal 316A. This mixed sum may be used for call progress monitoring through an external speaker. In addition, the relative levels of the DSP input and output signals 316A and 316B may be programmed through the interface 106.

FIG. 3C is a block diagram of an embodiment 352 in which voice mode operations are desired. The input 316B to the DSP circuitry 154 is connected to the isolation interface 164. The output 316A of the ~~DSP circuitry 316A~~ DSP circuitry 154 is combined with the DSP input 316B to provide an input 320B to the DAC 310. The analog out AOUT 214, therefore, is a combination of the DSP input signal 316B and the DSP output signal 316A. The ADC 312 takes the analog in AIN 216 and provides a digital signal 320A for the isolation interface input 316C. In this configuration for path control circuitry 306, the analog out AOUT 214 provides a voice output, and the analog in AIN 216 provides a voice input. In addition, the DSP circuitry 154 may process these signals, if the modem processor 404 of FIG. 4 is not being bypassed for PCM data mode.

For this voice mode of operation embodiment of FIG. 3C, voice information may be received through the analog in AIN connection 216, processed by the ADC 310 and sent across the isolation barrier 104. Looking to FIG. 5, it is seen that the DAC 504 may convert the digital voice information produced by ADC ~~310~~ 312 for transmission to the communication line interface 112. Also in voice mode, incoming voice signals from the communication line interface 112 may be converted to digital information by ADC 506 and sent across the isolation barrier 104.

The DAC 310 may then convert this digital voice information back to analog voice information and output it through the analog out AOUT connection 214.

FIG. 3D is a block diagram of an embodiment 354 in which test mode operations are desired. In this configuration for the path control circuitry 306, the DSP output signal 316A and the ~~DPS~~ DSP input signal 316B are connected together. These connections allow for the DSP circuitry to be more easily tested through the external interface 106. Similarly, the output 320A of the ADC 312 and the input 320B of the DAC 310 are connected together. These connections allow for the voice CODEC 152 to be more easily tested.

FIG. 3E is a block diagram of an embodiment 356 in which a CODEC mode of operation is desired. The DSP output signal 316A is connected to the isolation interface 164 and to the input 320B to the DAC 310. The analog out AOUT 214, therefore, is based upon the DSP output signal 316A. The ADC 312 converts the analog in AIN 216 and provides signal 320A as the DSP input signal 316B. This operational mode is helpful, for example, in voice prompting and speaker phones, and provides a stand-alone voice CODEC feature that may be accessed through the external interface 106. Thus, an on-chip voice CODEC 152 provides an optional analog input and output to the chip. Although the DAC 310 is connected to the analog out AOUT ~~pint 214,~~ pin 214 it is noted that the analog in AIN pin may be selected from among the general purpose ~~input/out~~ input/output pins GPIO1-4. The CODEC 152 also allows analog voice information to be sent across the isolation barrier 104 to the line-side line-isolation IC 102 and then to the telephone line.

In short, programmable path control circuitry 306 provides the ability for an external device to determine the data processing and data flow through the system-side line-isolation IC 100, as desired.

FIG. 4A is a diagram of a communication timing sequence that may be utilized to transmit raw data, such as pulse-code-modulated (PCM) data, to and from the system-side line-isolation IC 100. The line 478 represents the receive RXD or transmit TXD pins through which the information may be sent or received. This timing includes START bits 471 and 477, which are low logic levels for the embodiment in FIG. 4A, and STOP bits 475 and 479, which are high logic levels for the embodiment in FIG. 4A. The logic levels for the START bits 471, 477 and the STOP bits 475, 479 may be selected as desired. It is noted that PCM data may be used to represent voice information over phone lines.

In the embodiment shown, the raw PCM data ~~has be designed~~ has been designed to be 14-bit data (D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, and D13). This 14-bit data is represented by PCM data bits (D7-D13) 474 and PCM data bits (D0-D6) 476. These two sets of 7-bits of data may be sent to and from the DSP circuitry 154A and 154B in two 8-bit words. The first bits 470 and 472 of each 8-bit word are high/low byte flags. Thus, in the example shown in FIG. 4A, the low byte is indicated by a logic "0" in the first bit 470 of the first 8-bit word. The high byte is indicated by a logic "1" in the first bit 472 of the second 8-bit word. It is noted that these logic levels could be reversed if desired so that a logic "1" represented the low byte and a logic "0"

represented the high byte. In addition, the high data word 474 ~~and the low data word 476~~ 476 and the low data word 474 may be switched, if desired.

It is also noted that the 14-bit PCM data sample size is a design feature that may be modified as desired. In addition to the number of data bits, the number of data words and the number of flag bits may be adjusted as desired. For example, if more than two data words are utilized, a plurality of flag bits may be used for each data word to identify the order in which the data should be interpreted. Furthermore, the flag bits could be eliminated if the external device were designed to assume the order of the data words. Similarly, the start and stop bits could be eliminated if desired. Still further, a plurality of serial input pins or a plurality of serial output pins could be utilized so that the PCM data could be separated into multiple words and then be transmitted through the plurality of serial input/output pins at the same time. For example, for 14-bit PCM data, a 7-bit PCM data word could be sent or received through a first serial input/output pin at the same time a second 7-bit PCM data word was sent or received through a second serial input/output pin. It is recognized, therefore, that the data transfer protocol, including the number of pins utilized, may be modified as desired without departing from the present invention.

Using this technique, for example, an asynchronous interface may be used to send and receive raw PCM voice data. To provide this PCM voice data for a 9.6 kHz sample rate and 16-bit samples, a 192 kHz baud rate or greater is required through the interface 106 between the external device 202 and the system-side line-isolation IC 100.

To enter the raw data mode, the system-side line-isolation IC 100 may be given a command so that the modem processing provided by modem processor 404 is bypassed. Thus, raw data is sent and received through the interface 106. For data transmission of raw data from the system-side line-isolation IC 100 to the external microcontroller 202, the external microcontroller 202 may be assumed to have the speed to handle the data without need for a control signal. For data transmission of raw data from the external microcontroller 202 to the system-side line-isolation IC 100, the clear-to-send CTS_ pin 212 may be used to tell the external microcontroller when the system-side line-isolation IC 100 is ready for more data. It is noted that the protocol utilized for PCM data transfer may be designed and operated as desired.

By providing a technique for transmission of raw data, such as PCM data, the present invention accomplishes an advantageously simple interface for embedded modems with voice features.

FIG. 4B and FIG. 4C depict block diagrams of DSP circuitry 154A and 154B, respectively, for bypassing modem processor 404, if desired.

FIG. 4B is a block diagram for the receive path DSP circuitry 154A for the system-side line-isolation IC 100 of combined modem and line-isolation system 150 according to the present invention. DSP circuitry 154A includes a digital decimation filter 402, a modem processor 404, and a multiplexer 406. The data 316 entering the receive path DSP circuitry 154A will be in a

digital pulse density modulated data format from an analog-to-digital converter, for example ADC 312 or ADC 506. The digital decimation filter 402 converts this digital pulse density modulated data into, for example, pulse code modulated (PCM) data 410. The modem processor 404 may process this PCM data to produce modem data 414. Depending on the programmable control signal 412 applied to the MUX 406, output data 314 from the DSP 154A will either be raw digital PCM data 410 or processed modem data 414.

FIG. 4C is a block diagram for the transmit DSP path circuitry 154B for the system-side line-isolation IC 100 of the modem and line-isolation system according to the present invention. DSP circuitry 154B includes an interpolation filter 450, a digital modulator 452, a modem processor 404, and a multiplexer 454. The data 314 entering the transmit path DSP circuitry 154B will either be raw data, such as PCM data, or modem data provided through the communication interface 106. If data 314 is modem data, the modem processor 404 will convert this modem data to modem PCM data 457. Depending upon the programmable control signal 456 applied to the MUX 454, data 458 will either be raw PCM data 314 or processed modem PCM data 457. PCM data 458 is then processed by the interpolation filter 450 and the digital modulator 452 to produce data 316 that will be in a digital pulse density modulated format. This pulse density modulated data 316 may be output, for example, through the DAC 310 or the DAC 504.

FIG. 5 is a block diagram of an embodiment for the line-side line-isolation IC 102 of combined modem and line-isolation system, according to the present invention. The line-side

line-isolation IC 102 includes an isolation interface 166, a DAC 504, an ADC 506 and line interface circuitry 508. The isolation interface receives and sends data ~~across~~ through interface 110 across the isolation barrier 104. The interface circuitry 508 sends and receives data across the interface 112 to the communication line. The DAC 504 converts digital pulse density modulated data 510 to analog data 516. The ADC 506 converts analog data 514 to digital pulse density modulated data 512.

As described above with reference to FIGS. 1A and 1B, the external interface 106 may be an asynchronous serial interface. Thus, the UART 156 of the system-side line-isolation IC 100 may be an asynchronous serial receiver transmitter. However even though the UART is an asynchronous serial receiver transmitter, according to the techniques disclosed herein synchronous modem transmission protocols may be implemented through the UART 156. For example, one such type of synchronous modem transmission protocol is the HDLC (high-level data link control) protocol. In the HDLC protocol, data and control information may ~~by~~ be framed and is typically transmitted across a synchronous serial or parallel external interface. Thus in a typical prior art approach, information provided on a synchronous serial or parallel external interface is provided in a synchronous manner to HDLC framing circuitry which may be contained within a microcontroller of a modem DSP.

According to the techniques disclosed herein, data and control information of an HDLC protocol may be presented at the TXD and RXD pins through the UART 156 even though the UART 156 may be an asynchronous serial receiver transmitter. Thus, both transmit and receive

data transfers of a serial modem protocol may be implemented through an asynchronous serial interface. The HDLC framing may be performed within the microcontroller 151 that is coupled to the UART 156 as shown in FIG. 1B.

The HDLC protocol (or other synchronous protocols) may be selected by setting appropriate flags in registers of the system-side line-isolation IC through use of commands sent through the serial interface during command modes. The external microcontroller or other external interface circuitry (such as microcontroller 202 of FIG. 2A) may now send/receive data across the UART using either the ~~8-bit~~ 8-bit word or 9-bit word formats described above. The system-side line-isolation IC 100 may then begin framing data into the HDLC format. When no data is available from the external microcontroller 202, the HDLC flag pattern is sent repeatedly to the communication line 112. When data is available, the system-side line-isolation IC 100 computes the CRC (cyclical redundancy checking) code throughout the frame and the data is sent according to the HDLC protocol. When in the HDLC mode (or other synchronous protocols), data flow control for information sent through the RXD pin to the UART is sent in a similar manner to normal asynchronous flow control in that the clear to send pin CTS indicates when the system-side line-isolation IC 100 is ready to accept information. FIG. 6A is a timing diagram showing the data transfer to the RXD pin during the HDLC mode. As shown in FIG. 6A, the external interface circuitry may provide a frame N beginning at time 602 and a frame N+1 at time 604. At both times 602 and 604, the CTS_ line is low to indicate that the system-side line-isolation IC 100 is ready to accept information. When the system-side line-isolation IC is ready to accept additional information (such as time 608) but no word is received by the UART

through the RXD pin, the system-side line-isolation IC will recognize this as an end of frame, change the CTS_ signal, and calculate/send the CRC code. Thus, the system-side line-isolation IC determines an end of frame event based upon no frame data being received for some time period. As shown in FIG. 6A, an end of frame may be detected at time 609. HDLC CRC information may then be sent from the system-side line-isolation IC 100 to the communication line 112 after the end of frame has been determined. The CTS_ signal will again change at time 610 to again indicate that the system-side line-isolation IC 100 is ready to accept data on the RXD pin.

When transmitting HDLC data (or data in other synchronous protocols) from the asynchronous serial TXD pin to the external interface circuitry (such as microcontroller 202), end of frame information may be indicated to the external interface circuitry in different manners. In one approach, a general purpose control pin may be utilized as an end of frame (EOFR) indicator. For example, as shown in FIG. 1B the GPIO1 pin may be utilized as an EOFR indicator when in the HDLC mode. Thus, the external interface circuitry may monitor the GPIO1 pin to determine when an HDLC end of frame has occurred. In another approach, when 8 data bits are utilized with a ~~9-bit~~ 9-bit word format, a ninth control bit may be utilized to indicate an EOFR event. The ninth bit may be the same bit as described above with reference to the escape function. Thus, when receiving data on the RXD pin the ninth bit may indicate the escape function and when transmitting data (in HDLC or other synchronous protocols) on the TXD pin the ninth bit may indicate an EOFR event.

Thus, synchronous information may be sent to or from the asynchronous serial UART to the asynchronous interface by providing synchronous timing information to the external interface circuitry.. Exemplary approaches for providing this timing information may include utilizing a separate pin or utilizing additional bits combined with the data words. For example, the CTS pin may indicate timing information when data is being sent to the RXD pin, the GPIO1 pin may indicate timing information when data is being sent from the TXD pin or a designated bit of an n-bit word format may indicate timing information when data is being sent from the TXD pin. The exemplary approaches to provide the timing information are not meant to be limiting and other approaches may be utilized.

When the system-side line-isolation IC 100 is connected to a communication line 112 (through an isolation barrier 104 and line-side line-isolation IC 102) to receive HDLC information from the line that is to be transmitted on the TXD pin, the system-side line-isolation IC 100 detects the HDLC flag data. When non-flag data is detected, the CRC computing begins and data is sent from the UART to the TXD pin. A timing diagram for transmitting data on the TXD pin is shown in FIG. 6B. The data that the system-side line-isolation IC 100 receives from the communication line 112 that is to be transmitted on the TXD pin is shown at time 620 in FIG. 6B. When the stop flag is received by the system-side line-isolation IC 100 from the communication line 112, the two CRC bytes ~~may transmitted~~ may be transmitted on the TXD pin as shown in FIG. 6B. The EOFR pin or bit 9 of the ~~9-bit~~ 9-bit word format (or some other designated bit) may then change to a high state as shown at time 622 to indicate an end of frame event. While the EOFR pin or bit 9 is high, a control word such as a frame result word may be transmitted as indicated at

time 624. The frame result word may indicate the occurrence of a completed HDLC frame with correct CRC, the occurrence of a completed HDLC frame with a CRC error, the occurrence of an aborted HDLC frame, or some other framing result. Thus, data may be asynchronously sent on the TXD pin and if the EOFR pin (or bit 9) is low the data is valid frame data and if the EOFR pin (or bit 9) is high the data is frame result data.

Sending the frame result word to the external interface circuitry eliminates the need for the external interface circuitry to read registers within the system-side line-isolation IC to determine the status of the HDLC frames. In addition, it will be noted that the frame result word is sent after an HDLC stop flag is detected, thus, the frame result word is provided over the asynchronous serial interface at a time when no data is required to be transmitted at the TXD pin.

Further modifications and alternative embodiments of this invention will be apparent to those skilled in the art in view of this description. It will be recognized, therefore, that the present invention is not limited by these example arrangements. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the manner of carrying out the invention. It is to be understood that the forms of the invention herein shown and described are to be taken as the presently preferred embodiments. Various changes may be made in the shape, size and arrangement of parts. For example, equivalent elements may be substituted for those illustrated and described herein, and certain features of the invention may be utilized independently of the use of other features, all as would be apparent to one skilled in the art after having the benefit of this description of the invention.